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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,260	07/30/2003	Erin Antony Handgen	200205911-1	8717

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,260	HANDGEN ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 7 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 7, it is unclear what may be the "at least one additional integrated circuit component." Applicants are invited to point out to the specification, by page and line number, the disclosure of the "at least one additional integrated circuit component" as claimed.

In claim 11, the word "alternatively" renders the claim indefinite. The word "alternatively" means: a: The choice between two mutually exclusive possibilities, b: A situation presenting such a choice, or c: Either of these possibilities. However, as amended, there is only one configuration for each logic portion.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (Estakhri, 6,172,906).

As broadly drafted, these claims do not define any structure that differs from Estakhri.

With regard to claim 1, Estakhri discloses an integrated circuit component (shown generally at Figs. 1 and 6a) comprising: logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic block") capable of being configured to interface with a first companion integrated circuit (18/ or 670) and to receive information that is communicated from the first companion integrated circuit (18 or 670), which information was communicated to the first companion integrated circuit (18 or 670) via a first portion of a system bus (28/680); and logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic block") capable of being configured to interface with a second companion integrated circuit (20/672) and to receive information that is communicated from the second companion integrated circuit (20/672), which information was communicated to the second companion integrated circuit (20/672) via a second portion of the system bus (38/684). It is also clear in

Estakhri that the first companion integrated circuit (18/ or 670) and the second companion integrated circuit (20/672) are disposed in separate integrated circuit chips.

With regard to claim 2, it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both logic portions.

With regard to claim 3, it is clear that integrated circuit component further comprising functional logic (flash memory logic) for performing at least one logic operation (memory operation) for the integrated circuit component.

With regard to claim 4, it is clear that the system bus (680/684) is a point-to-point serial communication bus.

With regard to claim 5, it is clear that the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus (see at least column 7, lines 4-9).

With regard to claim 6, Estakhri discloses a system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component (shown generally at Fig. 1, 6(a, b) comprising: a host integrated circuit component (12/610/504) communicating with other integrated circuit components (16/506, for example) via a system bus (675); a first integrated circuit component (18/670) comprising logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic") for interfacing with a first portion (28/680) of system bus (275); a second integrated circuit component (20/672) comprising logic (since 506 is an digital IC

and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic") for interfacing with a second portion (38/684) of system bus (275); a third integrated circuit component (defined by flash storage 669 or 674) not directly coupled with the system bus (675) and comprising logic (it is clear flash memory operations must comprise "logic") for communicating with the host integrated circuit (14/610) via the first and second integrated circuit components (18/670 and 20/672). Estakhri further discloses a third integrated circuit component (defined by flash storage 669 or 674) not directly coupled with the system bus (675). It alsot is clear that the first and second integrated circuit components (18/670 and 20/672) as well as the third integrated circuit component (defined by flash storage 669 or 674) are provided in separate IC chips. A flash memory comprises flash controller and flash storage. The flash storage 669 or 674 is either Intel NOR chip or Toshiba NAND chip. Thus, it is clear that storage 669 or 674 is an IC chip itself and separate from IC chip 670 or 672. See also definition of flash memory by Wikipedia, cited below.

With regard to claim 8, it is clear that the third integrated circuit further comprising functional logic (memory operation logic, for example) that performs a conventional functional operation (memory operation).

With regard to claim 9, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins (it is clearly inherent that flash memory (669/674) must comprise pins for providing electrical connections and communication, see also NOR and NAND flash below) for channeling communications to a host

integrated circuit (14/610/504) through a first intermediate integrated circuit (18/670), the first intermediate integrated circuit (18/670) being in direct communication with the host integrated circuit via a first portion (28/680) of a system bus (275) ; and a second set of conductive pins for channeling communications to the host integrated circuit (14/610/504) through a second intermediate integrated circuit (20/672), the second intermediate integrated circuit (20/672) being in direct communication with the host integrated circuit (14/610/504) via a second portion (38/684) of the system bus. It is also clear in Estakhri that the integrated circuit component (shown generally at Figs. 1 and 6a), the first intermediate integrated circuit (18/ or 670), and the second intermediate integrated circuit (20/672) are disposed in separate integrated circuit chips.

With regard to claim 10, it is clear that the integrated circuit component further comprises unified bus logic (provided by controller 12/510) configured to consolidate information received from the channeled communications through the first and second set of conductive pins.

With regard to claim 11, Estakhri discloses an integrated circuit component comprising two independent logic portions (provided by chips 18/670 or 20/672), each logic portion being capable of being alternatively configured to communicate with a host integrated circuit (14/610/504) via a portion (28/680 or 38/684) of a system bus and a companion integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit (the other of 18/670 or 20/672), which information was communicated to the companion integrated circuit via a portion (28/680 or 38/684) of a system bus.

With regard to claim 12, the integrated circuit component further comprises unified bus logic (provided by controller 12/510) configured to consolidate information received from both logic portions.

Response to Arguments

Applicants' arguments filed 10/28/2005 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 Rejection:

Applicants argue that "the Office Action has taken certain inconsistent positions. As one example, the Office Action has rejected claim 6 under both 35 U.S.C. 112, second paragraph, as well as 35 U.S.C. 102 as allegedly anticipated by U.S. Patent 6,172,906." See Applicants' remark, page 6.

In response to Applicants' argument, MPEP 2173.06 clearly states that where the degree of uncertainty is not great, and where the claim is subject to more than one interpretation and at least one interpretation would render the claim unpatentable over the prior art, an appropriate course of action would be for the examiner to enter two rejections: (A) a rejection based on indefiniteness under 35 U.S.C. 112, second paragraph; and (B) a rejection over the prior art based on the interpretation of the claims which renders the prior art applicable. See, e.g., Ex parte Ionescu, 222 USPQ 537 (Bd. App. 1984).

With regard to claim 7, Applicants still have not provided any further response regarding "at least one additional integrated circuit component" as claimed in claim 7. It is unclear what may be the "at least one additional integrated circuit component not directly coupled with the system bus, and comprising logic for communicating with the host integrated circuit via the first, second, and third integrated circuit components." Applicants are invited to point out to the specification, by page and line number, and drawings, the disclosure of the "at least one additional integrated circuit component" as claimed.

The 102 Estakhri ('906) 102 Rejection:

Applicants argue that "claim 1 is directed to 'an integrated circuit component' (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of the system bus. Likewise, the second logic block is capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the bus. Simply stated, these features are not disclosed in the '906 patent."

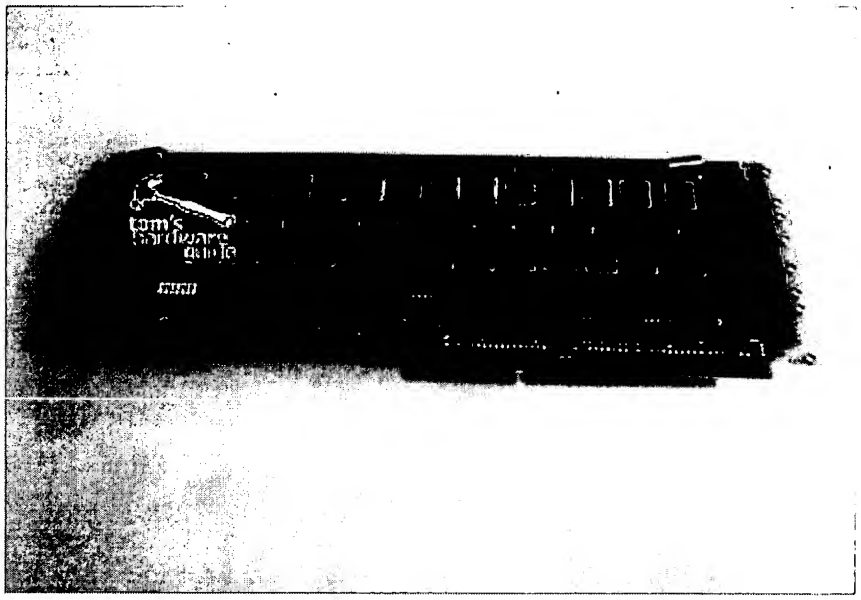
Contrary to Applicants' argument, Estakhri discloses an integrated circuit component (shown generally at Figs. 1 and 6a) comprising: logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic block") capable of being configured to interface with a first companion integrated circuit (18/ or 670) and to receive information that is communicated from the first companion integrated circuit (18 or 670), which information was communicated to the first companion integrated circuit (18 or 670) via a first portion of a system bus (28/680); and logic block (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 is readable as the so-called "logic block") capable of being configured

to interface with a second companion integrated circuit (20/672) and to receive information that is communicated from the second companion integrated circuit (20/672), which information was communicated to the second companion integrated circuit (20/672) via a second portion of the system bus (38/684). It is also clear in Estakhri that the first companion integrated circuit (18/ or 670) and the second companion integrated circuit (20/672) are disposed in separate integrated circuit chips.

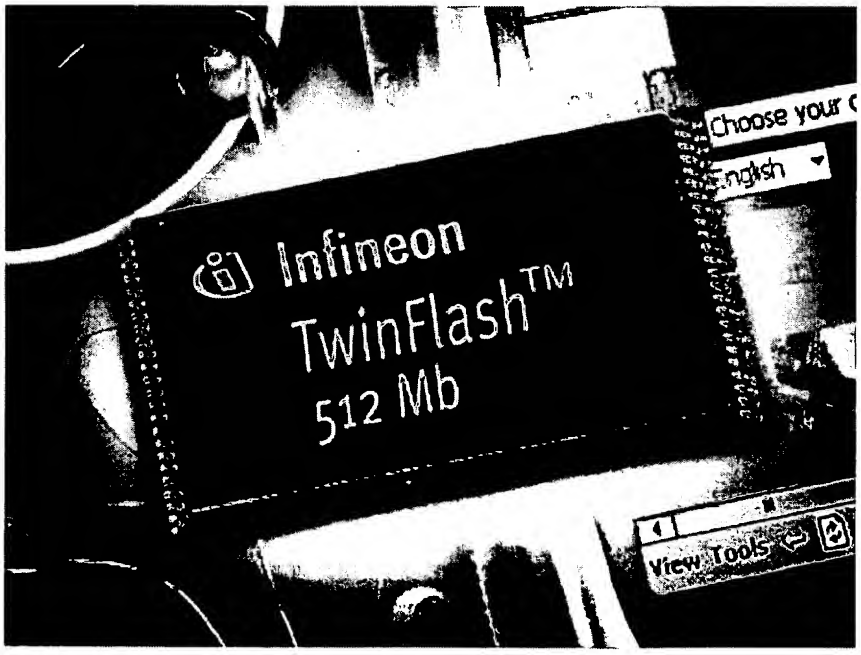
With regard to claim 6, Applicants argue that "the teachings of the '906 patent are not applicable to the embodiments defined by claim 6, as the '906 patent fails to disclose at least the third integrated circuit component. Specifically, claim 6 defines the first, second, and third integrated circuit components as comprising separate integrated circuit chips, and it is clear that the applied element (reference numeral 669 of the '906 patent) does not comprise a physically separate integrated circuit chip from reference numeral 670, which is applied as allegedly comprising the second integrated circuit component."

Contrary to Applicants' argument, Estakhri discloses a third integrated circuit component (defined by flash storage 669 or 674) not directly coupled with the system bus (675). Further, it is clear that the first and second integrated circuit components (18/670 and 20/672) as well as the third integrated circuit component (defined by flash storage 669 or 674) are provided in separate IC chips. A flash memory comprises flash controller and flash storage.

The flash storage 669 or 674 is either Intel NOR chip:



or Toshiba NAND chip:



Thus, it is clear that storage 669 or 674 is an IC chip itself and separate from IC chip 670 or 672. See also definition of flash memory by Wikipedia, cited below.

With regard to claim 9, Applicants argue that "there is no disclosure in the '906 patent of an integrated circuit that is coupled to a host integrated circuit via two intermediate integrated circuits." At the outset, it is noted that Applicants' argument is not specific to the claim language. In any event, contrary to Applicants' argument, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins (it is clearly inherent that flash memory (669/674) must comprise pins for providing electrical connections and communication, see also NOR and NAND flash above) for channeling communications to a host integrated circuit (14/610/504) through a first intermediate integrated circuit (18/670), the first intermediate integrated circuit (18/670) being in direct communication with the host integrated circuit via a first portion (28/680) of a system bus (275) ; and a second set of conductive pins for channeling communications to the host integrated circuit (14/610/504) through a second intermediate integrated circuit (20/672), the second intermediate integrated circuit (20/672) being in direct communication with the host integrated circuit (14/610/504) via a second portion (38/684) of the system bus. It is also clear in Estakhri that the integrated circuit component (shown generally at Figs. 1 and 6a), the first intermediate integrated circuit (18/ or 670), and the second intermediate integrated circuit (20/672) are disposed in separate integrated circuit chips.

In response to Applicants' argument regarding claim 11, Estakhri discloses an integrated circuit component comprising two independent logic portions (provided by chips 18/670 or 20/672), each logic portion being capable of being alternatively configured to communicate with a host integrated circuit (14/610/504) via a portion (28/680 or 38/684) of a system bus and a companion integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit (the other of 18/670 or 20/672), which information was communicated to the companion integrated circuit via a portion (28/680 or 38/684) of a system bus.

The Non-Statutory Double Patenting:

Applicants' Terminal Disclaimer filed 10/28/05 has been approved, and therefore, the non-statutory double patenting rejection is withdrawn.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Definition of "Flash Memory" from Wikipedia is cited.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner